IN THE SPECIFICATION:

Please replace paragraph **[0005]** with the following:

[0005] The liquid crystal display panel 3 is provided with a plurality of liquid crystal cells and thin film transistors (TFT's) for switching data signals to be applied to the liquid crystal cells. The plurality of liquid crystal cells and TFT's are arranged at intersections between a matrix array of data lines DL1 to [[DLn]] DLp and gate lines GL1 to GLm.

Please replace paragraph **[0006]** with the following:

[0006] The gate driving IC 2 includes multiple-stage shift registers for driving the gate lines GL1 to GLm, and responds to a gate start pulse GSP to sequentially drive the gate lines GL1 to [[GLn]] GLm. FIG. 2 is a waveform diagram of a gate pulse applied to each of the data lines shown in FIG. 1. The gate driving IC 2 sequentially applies a gate driving pulse to the m-number of gate lines GL1 to GLm on the liquid crystal display panel 3 when the gate start pulse GSP is applied to the gate driving IC 2, thereby sequentially driving the gate lines GL1 to GLm. Accordingly, the TFT's of the liquid crystal display panel 3 are sequentially driven for each individual gate line to sequentially apply the data signals.

Please replace paragraph **[0007]** with the following:

[0007] The data driving IC 1 includes shift registers and latches. The data driving IC 1 shifts data bits in response to a data shift clock DSC, and applies data to the data lines DL1 to [[DLn]] DLp simultaneously in response to a data output enable signal DOE. If the data output enable signal DOE is applied to the data driving IC 1, then the data driving IC 1 applies ~~n-number~~ p-number of

data signals to the ~~n-number~~ p-number of data lines DL1 to [[DLn]] DLp whenever a gate driving pulse is generated. The n-number of data signals generated from the data driving IC 1 have alternating polarities in accordance with an arranged sequence of adjacent data lines. In addition, the ~~n-number~~ p-number of data signals generated from the data driving IC 1 have alternating polarities converted with a lapse of frame.

Please replace paragraph **[0018]** with the following:

[0018] In another aspect, a driving apparatus for a liquid crystal display panel of dot inversion system having liquid crystal cells arranged at intersections between a plurality of data lines and a plurality of gate lines in a matrix array, includes a data driving integrated circuit supplying data to the data lines of the liquid crystal display panel, a gate driving integrated circuit responding to a gate start pulse to sequentially drive the gate lines of the liquid crystal display panel, and a pre-charging controller continuously generating first and second gate start pulses such that data corresponding to liquid crystal cells connected to an (n-2)th [[data]] gate line is supplied to liquid crystal cells connected to an nth [[data]] gate line, and applying the first and second gate start pulses to the gate driving integrated circuit.

Please replace paragraph **[0019]** with the following:

[0019] In another aspect, a device for driving a liquid crystal display panel having a plurality of data lines, a plurality of gate lines orthogonal to the plurality of data lines, and a plurality of liquid crystal cells, includes a data driving integrated circuit supplying data to the data lines, a gate driving integrated circuit responding to a gate start pulse to drive the gate lines, and a pre-

charging controller generating first and second gate start pulses to the gate driving integrated circuit, wherein data corresponding to liquid crystal cells connected to an (n-2)th [[data]] gate line is supplied to liquid crystal cells connected to an nth [[data]] gate line.

Please replace paragraph **[0034]** with the following:

[0034] The liquid crystal display panel 10 may be provided with a plurality of liquid crystal cells, and thin film transistors (TFT's) for switching the data signals that are applied to the liquid crystal cells. The plurality of liquid crystal cells and TFT's are arranged at intersections between data lines DL1 to [[DLn]] DLp and gate lines GL1 to GLm in a matrix array.

Please replace paragraph **[0035]** with the following:

[0035] The data driving IC 8 may include shift registers and latches. The data driving IC 1 shifts data bits in response to a data shift clock DSC, and applies data for the data lines DL1 to [[DLn]] DLp simultaneously in response to a data output enable signal DOE.

Please replace paragraph **[0036]** with the following:

[0036] The gate driving IC 9 may include multiple-stage shift registers for driving the gate lines GL1 to GLm. The gate driving IC 9 responds to first and second gate start pulses GSP from the pre-charging controller 11 to sequentially drive the gate lines GL1 to [[GLn]] GLm.

Please replace paragraph **[0037]** with the following:

[0037] The pre-charging controller 11 may continuously generate the first and second gate start pulses to supply liquid crystal cells connected to the nth [[data]] gate line (n is an integer) with data corresponding to liquid crystal cells connected to the (n-2)th [[data]] gate line. The pre-charging controller 11 may apply a pre-gate start pulse PRE-GSP to the gate driving IC 9 as a first gate start pulse GSP1 without any delay. Furthermore, the pre-charging gate controller 11 may delay the pre-gate start pulse PRE-GSP by a two-clock time period of a data output enable signal DOE to apply a second gate start pulse GSP2 following the first gate start pulse GSP1 to the gate driving IC 9.